Effect of Extreme Ultra-violate Radiation on Non-volatile Memories and High-k Devices

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In the part of high dielectric constant dielectrics, EUV radiation damage on high dielectric constant (high-k) dielectric is evaluated. According to the trend of IC industry, TiN is selected as the metal gate electrode. Three kinds of high-k dielectric are evaluated. They are HfO_2, HfSiO, and HfAlO. Simple metal-oxide-Si (MOS) capacitor structure was fabricated as shown in Fig.1.

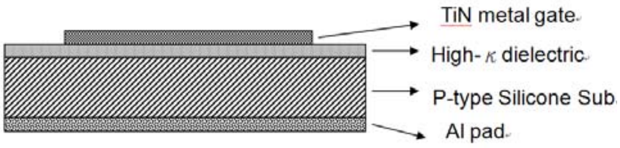
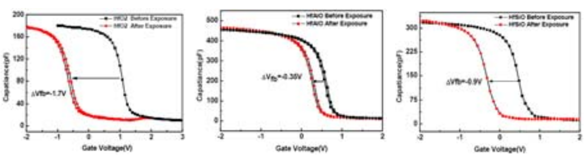


Fig. 1: Structure of the TiN(40nm)/high-κ(15nm)/Si-substrate MOS capacitor. The high-κdielectric is HfO_2, HfSiO, or HfAlO.

The starting material was 6-inch p-type Si substrate. After standard RCA clean process, various high-k dielectrics were depositedby a MOCVD system to a thickness of 15nm. The 40nm thick TiN metal gate was deposited by a sputter system and was patterned by RIE etching. After backside metallization, a 300 C/30 min alloy process finished the device fabrication.

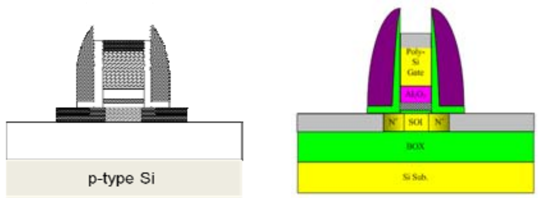


(a) (b) (c)

Fig. 2: C-V characteristics of the capacitors with (a) HfO2, (b) HfSiO, and (c) HfAlO dielectric before and after EUV exposure at 5x1012 photons/sec for 5 minutes.

Figures 2(a), 2(b), and 2(c) show the C-V characteristics of the samples with HfO2, HfSiO, and HfAlO, respectively, before and after EUV exposure for 5 min. The intensity of EUV light is 5x1012 photons/sec. Among these three kinds of high-k dielectric, HfAlO exhibits the best EUV resistance. The flat band voltage shifts (ΔVfb) of these three samples is -0.35V, -0.9V, and -1.7V in sequence. There is no C-V distortion. However, the hysteresis slightly increases. These observations indicate that HfAlO has the strongest immunity to EUV radiation damage, which may be due to the strong Al-O bond. Positive charges (hole traps) and border traps were generated during EUV exposure. Detailed analysis and reliability evaluating is under going.

In the part of non-volatile memory, the impact of EUV radiation on non-volatile memory (NVM) is evaluated. Two advanced NVM structures, silicon-oxide-nitride-silicon (SONOS) and nano-crystal (NC), are used. The device structures are shown in Fig.3



(a) (b)

Fig. 3: (a) Thin film transistor SONOS NVM with 4nm thick SiO2 tunneling layer 4nm, 7 nm thick Si3N4 trapping layer, and 20 nm thick SiO2 blocking layer . (b) Multi-gate TiN NC NVM with 4nm thick SiO2 tunneling layer, 7.5nm thick TiN/Al2O3 trapping layer, and 20nm Al2O3 blocking layer.

For the SONOS NVM, the memory performance degrades severely after EUV exposure. The memory window at high programming voltage reduces after exposure. The erase speed becomes lower and lower as the exposure time increases. The retention time also degrades and can not fulfill the 10 year requirement. Endurance test shows apparent window shrinkage after 1000 P/E operations as shown in Fig. 4(a). For the NC NVM, memory window, P/E speed, and retention do not affected apparently by EUV exposure. Figure 4(b) shows the endurance performance. The threshold voltage at both program and erase states shift downward after EUV exposure. However, the memory window dos not change after 100,000 P/E operations.

The better EUV radiation damage immunity of NC NVM than SONOS NVM can be understood by the difference in charge storage mechanism. SONOS use traps in the Si3N4 layer to store charges. EUV exposure may change the density as well as the energy level of these traps so that the memory performance charges apparently. However, for NC memory, charges are stored in NCs while the metallic NC will not be damaged by EUV, therefore, memory performance can be preserved.

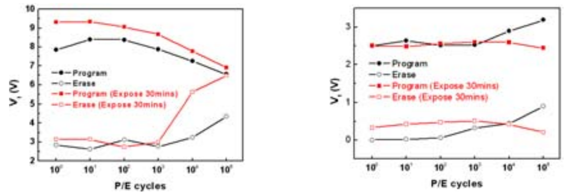


Fig. 4: Endurance performance of (a) SONOS NVM and (b) NC NVM before and after EUV exposure for 30 minutes.